AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An MPEG video decoding system, comprising:

a buffer configured to store an MPEG-formatted video signal or a DV-formatted video signal and to output a corresponding buffer output signal;

a VLD/IQ (Variable Length Decoder/Inverse Quantizer) device configured to perform a variable length decoding and an inverse quantization to the buffer output signal so as to generate a VLD/IQ output signal;

an IDCT (Inverse Discrete Cosine Transform) device configured to generate an IDCT transformed signal by

performing an 8×8 IDCT transform on the VLD/IQ output signal if the VLD/IQ output signal is the MPEG-formatted video signal, and

performing an 8×8 IDCT or a 4×8 IDCT transform on VLD/IQ output signal if VLD/IQ output signal is the DV-formatted video signal;

an adder; and

a motion compensator, wherein

if the IDCT transformed signal is an MPEG-formatted I-picture or a DV format signal,

the adder is configured to bypass and store the IDCT transformed signal into an external memory, and

if the IDCT transformed signal is an MPEG-formatted P-picture or an MPEG-formatted B-picture

the motion compensator is configured to

generate a motion compensated signal by performing motion compensation on a current frame based on motion information and a previous frame stored in the external memory, and

output the motion compensated signal to the adder, and

the adder is configured to

add the IDCT transformed signal and the motion compensated signal, and store the added signal into the external memory.

~~a buffer for storing an MPEG formatted video signal or a DV formatted video signal;~~

~~a VLD/IQ means for performing a variable length decoding and an inverse quantization to the video signal outputted from the buffer;~~

~~an IDCT means for selectively performing an 8×8 IDCT and a 4×8 IDCT according to the format of the inversely quantized signal;~~

~~an adder for bypassing and storing the output signal of the IDCT means into an external memory if the output signal of the IDCT means is an MPEG formatted I picture or a DV format, and for adding the IDCT ed signal and a motion compensated signal and storing the added signal into the external memory if the output signal of the IDCT means is an MPEG formatted P picture or an MPEG formatted B picture; and~~

~~a motion compensator for performing a motion compensation by using a motion information and a previous frame stored in the external memory and outputting the motion compensated signal to the adder if the output signal of the IDCT means is the MPEG formatted P picture or the MPEG formatted B picture.~~

2. (Currently Amended) The MPEG video decoding system of claim 1, wherein the IDCT ~~means~~ device includes:

a horizontal 8×1 IDCT unit configured to generate a horizontally transformed IDCT signal by performing an 8×1 IDCT transform on the inversely quantized video signal in a horizontal direction;

a transverse buffer configured to perform a horizontal-vertical transposition to the horizontally transformed IDCT signal and to output a corresponding transverse buffer output signal;

a switching unit configured to control an output path of the signal outputted from the transverse buffer according to the format type of the inputted signal, and to output a corresponding switch output signal;

a vertical 8×1 IDCT unit configured to perform an 8×1 IDCT transform on the switch output signal in a vertical direction; and

a vertical 4×1 IDCT unit configured to perform a 4×1 IDCT transform on the switch output signal in a vertical direction.

~~a horizontal 8×1 IDCT unit for performing an 8×1 IDCT to the inversely quantized video signal in a horizontal direction;~~

~~a transverse buffer for performing a horizontal vertical transposition to the horizontally IDCT-ed signal;~~

~~a switching unit for controlling an output path of the signal outputted from the transverse buffer according to the format type of the inputted signal;~~

~~a vertical 8×1 IDCT unit for performing an 8×1 IDCT to the output signal of the switching unit in a vertical direction; and~~

~~a vertical 4×1 IDCT unit for performing a 4×1 IDCT to the output signal of the switching unit in a vertical direction.~~

3. (Original) The MPEG video decoding system of claim 2, wherein the format type of the inputted signal is one of

an MPEG format,

a vertical frame DCT of 625-50 DV format,

a vertical frame DCT of 525-60 DV format, and

a vertical field DCT of 525-60 DV format.

4. (Currently Amended) The MPEG video decoding system of claim 3, wherein

if the format type of the inputted signal is the MPEG format, the vertical frame DCT of 625-50 DV format and the vertical frame DCT of 525-60 DV format, the switching unit is configured to output the transverse buffer output signal~~outputs an output signal of the transverse buffer~~ to the 8×1 IDCT unit, and

if the format type of the inputted signal is the vertical field DCT of 525-60 DV format, the switching unit is configured to output the transverse buffer output signal ~~outputs the output signal of the transverse buffer~~ to the 4×1 IDCT.

5. (Currently Amended) The MPEG video decoding system of claim 1, further comprising:

a format converter, wherein the format converter ~~converts~~ is configured to

convert a video-decoded 4:2:0 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is the MPEG format or a 625-50 DV format, and

~~converts~~ convert a video-decoded 4:1:1 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is a 525-60 DV format.

6. (Currently Amended) The MPEG video decoding system of claim 1, further comprising:

a de-shuffler, wherein if the video-decoded signal is a 525-60 DV format, the de-shuffler is configured to

output the video-decoded signal as a super block unit comprising a plurality of macro blocks,

~~outputs the video-decoded signal by supper block unit consisting of a plurality of macro blocks, performs a de-shuffling to~~

deshuffle the video-decoded signal in order to reconfigure an original screen, and

~~stores~~ store the de-shuffled signal into the external memory.

7. (Currently Amended) An MPEG video decoding system including a memory interface for controlling data input/output between a video decoder and an external memory, the MPEG video decoding system comprising:

an MPEG system decoder configured to divide an external input MPEG bitstream into a video bitstream and an audio bitstream, and to output a corresponding MPEG system decoder output signal;

a DV (Digital Video) system decoder configured to

convert an external input DV formatted signal into a DIF (Digital Interface Format) signal,

divide the DIF signal into a video DIF and an audio DIF, and

output a corresponding DV system decoder output signal;

a single combined DV/MPEG video decoder configured to

receive the MPEG system decoder output signal and the DV system decoder output signal as a DV/MPEG video decoder input signal,

share a plurality of internal blocks to decode both the MPEG system decoder output signal and the DV system decoder output signal to generate decoded data, and

store the decoded data into the external memory; and

a format converter configured to perform a format conversion to generate a color difference signal, the color difference signal being a signal that is video-decoded by the combined DV/MPEG video decoder and outputted through the external memory,

wherein the single combined DV/MPEG video decoder is further configured to

perform an 8×8 IDCT if the DV/MPEG video decoder input signal is the MPEG system decoder output signal, and

perform an 8×8 IDCT or a 4×8 IDCT if the DV/MPEG video decoder input signal is the DV system decoder output signal.

~~an MPEG system decoder for dividing an external input MPEG bitstream into a video bitstream and an audio bitstream;~~

~~a DV system decoder for converting an external input DV formatted signal into a DIF signal and dividing the DIF signal into a video DIF and an audio DIF;~~

~~a single combined DV/MPEG video decoder for sharing a plurality of internal blocks to decode both the MPEG video signal outputted from the MPEG system decoder and the video DIF signal outputted from the DV system decoder and storing the decoded data into the external memory; and~~

~~a format converter for performing a format conversion to a color difference signal, the color difference signal being a signal that is video decoded by the combined DV/MPEG video decoder and outputted through the external memory.~~

8. (Original) The MPEG video decoding system of claim 7, wherein the MPEG bitstream is inputted to the MPEG system decoder through a tuner, and the DV formatted signal is inputted to the DV system decoder through an IEEE-1394 interface.

9. (Currently Amended) The MPEG video decoding system of claim 7, wherein the combined DV/MPEG video decoder includes:

a buffer configured to temporarily store and then output one of the MPEG system decoder output signal and the DV decoder output signal;

~~a buffer for temporarily storing a video signal outputted from one of the MPEG system decoder and the DV system decoder;~~

a VLD/IQ device configured to perform a variable length decoding and an inverse quantization of the video signal outputted from the buffer;

~~a VLD/IQ means for performing a variable length decoding and an inverse quantization to the video signal outputted from the buffer;~~

~~an IDCT means for~~

an IDCT device configured to generate an IDCT transformed signal by

performing an 8×8 IDCT if the inversely quantized signal is an MPEG format or 625-50 DV format, and

performing one of an 8×8 IDCT and [[an]] a 4×8 IDCT according to a DCT type if the inversely quantized signal is a 525-60 DV format;

an adder; and

a motion compensator, wherein

if the IDCT transformed signal is an MPEG-formatted I-picture or a DV format signal,

the adder is configured to bypass and store the IDCT transformed signal into an external memory, and

if the IDCT transformed signal is an MPEG-formatted P-picture or an MPEG-formatted B-picture

the motion compensator is configured to

generate a motion compensated signal by performing motion compensation on a current frame based on motion information and a previous frame stored in the external memory, and

output the motion compensated signal to the adder, and

the adder is configured to

add the IDCT transformed signal and the motion compensated signal, and store the added signal into the external memory.

~~an adder for bypassing and storing the output signal of the IDCT means into an external memory if the output signal of the IDCT means is an MPEG formatted I picture or a DV format, and adding the IDCT-ed signal and a motion compensated signal and storing the added signal into the external memory if the output signal of the IDCT means is an MPEG formatted P-picture or an MPEG formatted B picture; and~~

~~a motion compensator for performing a motion compensation by using a motion information and a previous frame stored in the external memory, and outputting the motion compensated signal to the adder if the output signal of the IDCT means is the MPEG formatted P-picture or the MPEG formatted B picture.~~

10. (Currently Amended) The MPEG video decoding system of claim 9, wherein the IDCT ~~means~~ device includes:

a horizontal 8×1 IDCT unit configured to generate a horizontally IDCT transformed signal by performing an 8×1 IDCT transform on the inversely quantized video signal in a horizontal direction;

~~a horizontal 8×1 IDCT unit for performing an 8×1 IDCT to the inversely quantized video signal in a horizontal direction;~~

a transverse buffer configured to perform a horizontal-vertical transposition to the horizontally IDCT transformed signal and to output a corresponding transposed signal;

~~a transverse buffer for performing a horizontal vertical transposition to the horizontally IDCT-ed signal;~~

a switching unit configured to control an output path of the transposed signal according to the format type of a switching unit input signal and to generate a corresponding switching unit output signal;

~~a switching unit for controlling an output path of the signal outputted from the transverse buffer according to the format type of an inputted signal;~~

a vertical 8×1 IDCT unit configured to perform an 8×1 IDCT transform on the switching unit output signal in a vertical direction to generate a vertically IDCT transformed signal; and

~~a vertical 8×1 IDCT unit for performing an 8×1 IDCT to the output signal of the switching unit in a vertical direction; and~~

a vertical 4×1 IDCT unit configured to perform a 4×1 IDCT transform on the vertically IDCT transformed signal.

~~a vertical 4×1 IDCT unit for performing a 4×1 IDCT to the output signal of the switching unit in a vertical direction.~~

11. (Currently Amended) The MPEG video decoding system of claim 10, wherein if the format type of the inputted signal is the MPEG format, a vertical frame DCT of 625-50 DV format and the vertical frame DCT of 525-60 DV format, the switching unit ~~outputs~~

is configured to output the transposed signal~~an output signal of the transverse buffer~~ to the 8×1 IDCT unit, and

if the format type of the inputted signal is a vertical field DCT of 525-60 DV format, the switching unit ~~outputs~~ is configured to output the transposed signal~~output signal of the transverse buffer~~ to the 4×1 IDCT.

12. (Currently Amended) The MPEG video decoding system of claim 7, wherein the format converter ~~converts~~ is configured to

convert a video-decoded 4:2:0 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is the MPEG format or a 625-50 DV format, and

~~converts~~ convert a video-decoded 4:1:1 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is a 525-60 DV format.

13. (Currently Amended) The MPEG video decoding system of claim 7, wherein if the video-decoded signal is a 525-60 DV format, the de-shuffler ~~outputs~~ is configured to

output the video-decoded signal by super block unit comprising a plurality of macro blocks,

deshuffle the video-decoded signal in order to reconfigure an original screen, and

store the de-shuffled signal into the external memory.

~~the video decoded signal by supper block unit consisting of a plurality of macro blocks, performs a de shuffling to the video decoded signal in order to reconfigure an original screen, and stores the de shuffled signal into the external memory.~~

14. (New) An MPEG video decoding method, comprising:

outputting a buffered video signal, the buffered video signal being one of an MPEG-formatted video signal and a DV-formatted video signal;

performing a variable length decoding and an inverse quantization on the output buffered video signal so as to generate a VLD/IQ output signal;

generating an IDCT transformed signal by

performing an 8×8 IDCT transform on the VLD/IQ output signal if the VLD/IQ output signal is the MPEG-formatted video signal, and

performing an 8×8 IDCT or a 4×8 IDCT transform on the VLD/IQ output signal if the VLD/IQ output signal is the DV-formatted video signal;

if the IDCT transformed signal is an MPEG-formatted I-picture or a DV format signal, bypassing and storing the IDCT transformed signal into an external memory; and

if the IDCT transformed signal is an MPEG-formatted P-picture or an MPEG-formatted B-picture

generating a motion compensated signal by performing motion compensation on a current frame based on motion information and a previous frame stored in the external memory, and

adding the IDCT transformed signal and the motion compensated signal, and storing the added signal into the external memory;

15. (New) An MPEG video decoding method for a system including a memory interface for controlling data input/output between a video decoder and an external memory, the MPEG video decoding method comprising:

dividing an external input MPEG bitstream into a video bitstream and an audio bitstream and outputting a corresponding MPEG system decoder output signal to a single combined DV/MPEG video decoder;

converting an external input DV formatted signal into a DIF (Digital Interface Format) signal, dividing the DIF signal into a video DIF and an audio DIF, and outputting a corresponding DV system decoder output signal to the single combined DV/MPEG video decoder;

receiving an input signal into the single combined DV/MPEG video decoder, the input signal being the MPEG system decoder output signal and the DV system decoder output signal, generating decoded data by sharing a plurality of internal blocks of the single combined DV/MPEG video decoder to decode both the MPEG system decoder output signal and the DV system decoder output signal, and storing the decoded data into the external memory; and

performing a format conversion to generate a color difference signal, the color difference signal being a signal that is video-decoded by the single combined DV/MPEG video decoder,

wherein the step of generating decoded data comprises

performing an 8×8 IDCT if the DV/MPEG video decoder input signal is the MPEG system decoder output signal, and

performing an 8×8 IDCT or a 4×8 IDCT if the DV/MPEG video decoder input signal is the DV system decoder output signal.